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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,361	07/30/2001	Steven C. Woo	RB1-026US	2536

29150 7590 04/09/2003

LEE & HAYES, PLLC
421 W. RIVERSIDE AVE, STE 500
SPOKANE, WA 99201

EXAMINER
VERBRUGGE, KEVIN

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,361	WOO ET AL.	
	Examiner	Art Unit	
	Kevin Verbrugge	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-8, 10, 11, 12, 14-19, 21, 23-26, 28, 29, 31, 32, 34-38, 40-43, and 45-51 are rejected under 35 U.S.C. 102(b) as being anticipated by "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa.

Regarding claims 1, 4, 5, 11, 14, 15, 16, 19, 25, 26, 32, 35, 36, 37, 38, 41, and 49, Ohsawa discloses the claimed plurality of dynamically refreshable memory cells as the DRAM cell array in Fig. 5.

He shows the claimed dynamically changeable use registers corresponding to groups of memory cells as refresh flags, shown in Figs. 4 and 5.

His memory device is configured to omit refreshing of memory cells that are not in use, as claimed, as indicated by the refresh flags.

Regarding claims 2 and 12, in section 4.3, last paragraph, Ohsawa mentions static mode which is the claimed self-refresh mode.

Regarding claims 6, 17, 21, 28, 34, 40, 46, and 48, Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

Regarding claims 7 and 42, Ohsawa's row of memory cells is a set of memory cells.

Regarding claims 8, 18, 24, 29, and 43, Ohsawa's refresh flags refer to rows as claimed.

Regarding claims 10 and 45, a page of memory cells is the same as a row of memory cells.

Regarding claims 23 and 31, Ohsawa shows his use registers in the memory devices in Figs. 4, 5, 7, and 8.

Regarding claims 47, 50, and 51, in Ohsawa's device, if all rows in a memory were cached (assuming the cache were large enough to hold all rows of a memory), then the whole memory would be placed in a reduced power mode since it would not be refreshed at all.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 9, 13, 20, 22, 27, 30, 33, 39, 44, 47, 50, 51, 52, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa.

Regarding claims 3, 13, 20, 27, 33, 39, 52, and 53, Ohsawa does not disclose the claimed recent-access flags he shows in-use registers (refresh flags) in Figs. 4 and 5 and refresh counters in Fig. 7.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed recent-access flags since Ohsawa's goal is to have the fewest refresh cycles possible and one way to reduce the number of refresh cycles is to not perform refreshes when a line has recently been refreshed as a result of a read or write. Ohsawa mentions these reads and writes as loads and stores at section 3.1, third paragraph.

Regarding claims 9 and 44, Ohsawa's refresh flags refer to rows. However, It would have been obvious to one of ordinary skill in the art at the time the invention was

made to use refresh flags for a bank since this would allow an entire bank to be shutdown if its refresh flag were not set, avoiding the need to read the refresh flag of each row.

Regarding claims 22 and 30, Ohsawa shows that his use registers are in the memory devices, however, It would have been obvious to one of ordinary skill in the art at the time the invention was made to move the use registers to the memory controller to have more centralized control over the memory cells. Putting the use registers in the memory controller would speed up access to them.

Regarding claims 47, 50, and 51, Ohsawa does not actually mention that when all rows of a memory are cached that the memory is placed in a reduced power mode, but It would have been obvious to one of ordinary skill in the art at the time the invention was made to place such a memory in a reduced power mode (such as the static mode mentioned by Ohsawa at section 4.3, last paragraph) to perhaps save even more power than by not refreshing any of the rows in the memory device.

Conclusion

The method claims are grouped and rejected with the apparatus claims because the steps of the method are met by the disclosure of the apparatus and methods of the reference(s) as discussed above.

Any inquiry concerning this or an earlier communication from the Examiner should be directed to Primary Examiner Kevin Verbrugge by phone at (703) 308-6663.

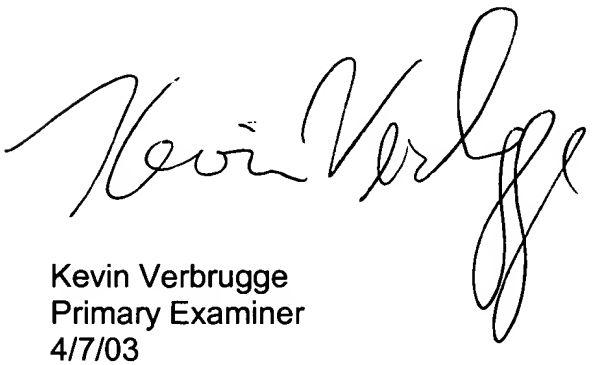
Any response to this action should be mailed to Commissioner for Patents, Washington, D.C. 20231 or faxed to

(703) 746-7238 After-final

(703) 746-7239 Official

(703) 746-7240 Non-Official/Draft

and labeled appropriately (After-final, Official, Non-Official/Draft). Hand-delivered responses should be brought to Crystal Park 2, 2121 Crystal Drive, Arlington, VA, 4th Floor (Receptionist).



Kevin Verbrugge
Primary Examiner
4/7/03